REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 1-14 are pending in this application. Claim 1 is amended and Claim 14 is added by the present response.

In the outstanding Office Action, Claims 1-8, 12 and 13 were rejected under 35 U.S.C. § 102(e) as being anticipated by Hosono et al. (U.S. Pub. No. US 2003/0214853, herein "Hosono"). Claims 9-11 were objected to as dependent upon a rejected base claim, but were noted as allowable if rewritten in independent form to include all of the limitations of their base claim and any intervening claims.

Initially, Applicants gratefully acknowledge the early indication of the allowable subject matter in Claims 9-11. However, since Applicants consider that amended Claim 1 patentably defines over the cited art, Claims 9-11 have presently been maintained in dependent form.

In response to the rejection of Claims 1-8, 12 and 13, Claim 1 has been amended to clarify the claimed invention. To that end, amended Claim 1 states that the plurality of memory cell arrays arranged in a matrix are located independently of each other. The changes to Claim 1 and Claim 14 are believed to find support in the disclosure as originally filed at least at Fig. 3 and page 12, line 3, to page 13 line 6, and thus are not believed to raise a question of new matter.

Claim 1 describes a semiconductor memory comprising "a plurality of memory cell arrays having a plurality of memory cells or memory cell units which includes a plurality of memory cells, arranged in a matrix, wherein the plurality of memory cell arrays are located independently of each other and have a plurality of cell array groups each of which includes two or more memory cell arrays, and a first Pass/Fail signal indicative of success or failure of an operation is outputted in accordance with each cell array group."

Applicants respectfully traverse the assertion in the outstanding Office Action that Hosono describes "a first Pass/Fail signal (the verify signal of erratic program verify) indicative of success or failure of an operation is outputted in accordance with each cell array group."[1] Hosono describes a semiconductor memory device with a plurality of memory cell arrays[2] which are connected to a single word line.[3]

The memory cell arrays described in the claims, however, differ from those of Hosono in that, as recited in Claim 1, "the plurality of memory cell arrays are located independently of each other." The memory cell arrays described in Hosono are not independent as they are connected to a single word line. In Hosono, a single word line connects the source gates (SG1) and a single word line connects the control gates (WL1) of each of the memory cells.[4] Therefore, the memory cell arrays described in Claim 1 and 14 are independent as the "plural word lines [are] connected to respective plural source gates and control gates of the plurality of memory cell arrays."[5] Thus, instead of all of the memory cells being connected to one word line, as is described in Hosono, Claims 1 and 14 recite independent memory cell arrays (Claim 1) connected to respective word lines (Claim 14).

Accordingly, Applicants respectfully submit that Hosono does not teach or suggest "a plurality of memory cell arrays having a plurality of memory cells or memory cell units which consists of a plurality of memory cells, arranged in a matrix, wherein the plurality of memory cell arrays are located independently of each other," as recited in Claim 1.

Therefore, it is respectfully submitted that independent Claim 1 and Claims 2-13 depending therefrom, are allowable.

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[1] Office Action, dated 7/25/2005.
[2] Hosono, Fig 2 (block B1, B2 or memory cells)
[3] Hosono, paragraph [0046] and [0122].
[4] Hosono, paragraph [0046].
[5] Claim 14.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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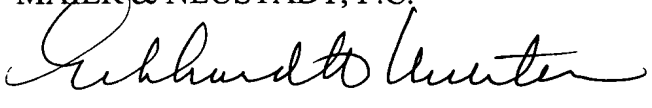

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